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PTO/SB/08A (08-00)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10691013
		Filing Date	10/20/2003
		First Named Inventor	Madurawe, Raminda U.
		Group Art Unit	
		Examiner Name	
Sheet 1 of 2	Attorney Docket Number		

U.S. PATENT DOCUMENTS						
Examiner Initials *	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
L		4,609,986		Hartmann et al.	09/02/1986	
		4,706,216		Carter	11/10/1987	
		4,761,768		Tumer et al.	08/02/1988	
		4,870,302		Freeman	09/26/1989	
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		5,844,422		Trimberger et al.	12/01/1998	
		6,134,173		Cliff et al.	10/17/2000	
		6,239,613		Reddy et al.	05/29/2001	
		6,275,065		Mendel	08/04/2001	
		6,448,808		Young et al.	09/10/2002	
		6,515,511		Sugibayashi et al.	02/04/2003	

FOREIGN PATENT DOCUMENTS							
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		Group Art Unit	
		Examiner Name	
		Attorney Docket Number	
Sheet	2	of	2

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
he		SEALS & WHAPSHOTT, "Programmable Logic – PLDs and FPGAs", 1997, pp 102-117, McGraw-Hill, USA	<input type="checkbox"/>
he		ASHOK K. SHARMA, "Programmable Logic Handbook – PLDs, CPLDs, & FPGAs", 1998, pp 99-171, McGraw-Hill, USA	<input type="checkbox"/>
he		V. BETZ, J. ROSE, A. MARQUARDT, "Architecture and CAD for Deep-Submicron FPGAs", Feb 1999, Kluwer Academic Publishers, Boston	<input type="checkbox"/>
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